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11/11/2003

Paul A. Farrar

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EXAMINER

NADAV, ORI

ART UNIT

PAPER NUMBER

2811

DATE MAILED: 10/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/705,185

Applicant(s)

FARRAR ET AL.

Examiner

ori nadav

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 29 June 2004.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-21 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 11 November 2003 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 11/11/03, 12/4/03.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## **DETAILED ACTION**

### ***Specification***

The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: Description for a device comprising a capacitor and a plurality of substantially parallel buried conductive elements, as recited in claim 1, for conductive elements including a material with a high melting point that prevents unwanted metallurgical changes, as recited in claims 2 and 11, for a metal comprises one of tungsten and a tungsten alloy, as recited in claims 4 and 18, for a first buried layer including a plurality of substantially parallel first conductive elements oriented in a first direction, a second buried layer including a plurality of substantially parallel second conductive elements oriented in a second direction, a second depth being greater than the first depth, and a deep trench capacitor formed between the plurality of substantially parallel first conductive elements, as recited in claims 8 and 15, for first buried layer and the second buried layer being substantially parallel to the active semiconductor layer, as recited in claim 9, for plurality of substantially parallel second conductive elements being connected to conductive parts that extend upwardly on opposite sides of the first buried layer beyond the first depth adjacent outer ones of the plurality of substantially parallel first conductive elements, as recited in claims 12 and 20, for plurality of substantially parallel second conductive elements are located either in front of or behind the deep trench capacitor, as recited in claim 15, for active device layer includes integrated circuits adapted for use with at least one of the group consisting of: dynamic

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random-access memory (DRAM), static random-access-memory (SRAM), flash memory, synchronous dynamic random-access-memory (SDRAM), extended-data-out random-access-memory (EDO RAM), and burst-extended-data-out random-access-memory (BEDO RAM), as recited in claim 16, for metal comprises one of a non-radioactive element selected from groups IVB, VB, VIB, VIIB, and VIIIB of the periodic table, and an alloy of the non-radioactive element, as recited in claim 19, and for a second direction is orthogonal to the first direction, as recited in claim 21.

### ***Drawings***

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, a plurality of substantially parallel buried conductive elements, as recited in claim 1, for conductive elements including a material with a high melting point that prevents unwanted metallurgical changes, as recited in claims 2 and 11, for a metal comprises one of tungsten and a tungsten alloy, as recited in claims 4 and 18, for a first buried layer including a plurality of substantially parallel first conductive elements oriented in a first direction, a second buried layer including a plurality of substantially parallel second conductive elements oriented in a second direction, a second depth being greater than the first depth, and a deep trench capacitor formed between the plurality of substantially parallel first conductive elements, as recited in claims 8 and 15, for first buried layer and the second buried layer being substantially parallel to the active semiconductor layer, as

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recited in claim 9, for plurality of substantially parallel second conductive elements being connected to conductive parts that extend upwardly on opposite sides of the first buried layer beyond the first depth adjacent outer ones of the plurality of substantially parallel first conductive elements, as recited in claims 12 and 20, for plurality of substantially parallel second conductive elements are located either in front of or behind the deep trench capacitor, as recited in claim 15, for active device layer includes integrated circuits adapted for use with at least one of the group consisting of: dynamic random-access memory (DRAM), static random-access-memory (SRAM), flash memory, synchronous dynamic random-access-memory (SDRAM), extended-data-out random-access-memory (EDO RAM), and burst-extended-data-out random-access-memory (BEDO RAM), as recited in claim 16, for metal comprises one of a non-radioactive element selected from groups IVB, VB, VIB, VIIB, and VIIIB of the periodic table, and an alloy of the non-radioactive element, as recited in claim 19, and for a second direction is orthogonal to the first direction, as recited in claim 21, must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate

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changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### ***Claim Rejections - 35 USC § 112***

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-21 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The embodiment of figure 1(b) discloses a capacitor 120 is formed between two buried conductors 114. There is no support in the embodiment of figure 1(b) for a plurality of substantially parallel buried conductive elements, as recited in claim 1, for conductive elements including a material with a high melting point that prevents unwanted metallurgical changes, as recited in claims 2 and

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11, for a metal comprises one of tungsten and a tungsten alloy, as recited in claims 4 and 18, for a first buried layer including a plurality of substantially parallel first conductive elements oriented in a first direction, a second buried layer including a plurality of substantially parallel second conductive elements oriented in a second direction, a second depth being greater than the first depth, and a deep trench capacitor formed between the plurality of substantially parallel first conductive elements, as recited in claims 8 and 15, for first buried layer and the second buried layer being substantially parallel to the active semiconductor layer, as recited in claim 9, for plurality of substantially parallel second conductive elements being connected to conductive parts that extend upwardly on opposite sides of the first buried layer beyond the first depth adjacent outer ones of the plurality of substantially parallel first conductive elements, as recited in claims 12 and 20, for plurality of substantially parallel second conductive elements are located either in front of or behind the deep trench capacitor, as recited in claim 15, for active device layer includes integrated circuits adapted for use with at least one of the group consisting of: dynamic random-access memory (DRAM), static random-access-memory (SRAM), flash memory, synchronous dynamic random-access-memory (SDRAM), extended-data-out random-access-memory (EDO RAM), and burst-extended-data-out random-access-memory (BEDO RAM), as recited in claim 16, for metal comprises one of a non-radioactive element selected from groups IVB, VB, VIB, VIIB, and VIIIB of the periodic table, and an alloy of the non-radioactive element, as recited in claim 19, and for a second direction is orthogonal to the first direction, as recited in claim 21.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okumura (4,912,535).

Okumura teaches in figures 6 and 7 and related text a semiconductor device comprising:

a doped silicon substrate 3 having an active semiconductor layer 9 formed thereon;

a conductive element 1 separated from the active semiconductor layer 9 by and surrounded by an oxide insulating material 24, 10b, 14; and

a deep trench P+ silicon capacitor 6 formed through the active semiconductor layer (see figure 5G), the insulative material, and between conductive elements, the deep trench capacitor surrounded by a dielectric material 7.

Okumura does not disclose in the embodiment of figure 6 a plurality of substantially parallel buried conductive elements. Okumura teaches a memory device comprises plurality of bit lines (column 1, lines 18-19).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form a plurality of substantially parallel buried conductive elements in Okumura's device in order to form a practical memory device (by forming

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plurality of bit lines) and in order to simplify the processing steps of making the device (by forming parallel bit lines), respectively.

Regarding claims 2-4, 11 and 17-18, Okumura teaches conductive elements include a material with a high melting point that prevents unwanted metallurgical changes, wherein the conductive elements are formed from a metal. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a metal comprises one of tungsten and a tungsten alloy in Okumura's device in order to reduce the contact resistance of the device.

Regarding claims 8, 12, 15 and 20, Okumura teaches

a first buried layer 1 buried at a first depth within the substrate and including a plurality of substantially parallel first conductive elements (bit lines) oriented in a first direction;

a second buried layer 1 buried at a second depth within the substrate and including a plurality of substantially parallel second conductive elements (bit lines) oriented in a second direction, wherein the second depth is greater than the first depth (since part of the bit line is deeper than other parts of the bit line), wherein the plurality of substantially parallel second conductive elements are connected to conductive parts that extend upwardly on opposite sides of the first buried layer beyond the first depth adjacent outer ones of the plurality of substantially parallel first conductive elements.

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Regarding claims 16 and 19-20, Okumura teaches the active device layer includes integrated circuits adapted for use with at least one of the group consisting of: dynamic random-access memory (DRAM), static random-access-memory (SRAM), flash memory, synchronous dynamic random-access-memory (SDRAM), extended-data-out random-access-memory (EDO RAM), and burst-extended-data-out random-access-memory (BEDO RAM), wherein the metal comprises one of a non-radioactive element selected from groups IVB, VB, VIB, VIIB, and VIIIB of the periodic table, and an alloy of the non-radioactive element, wherein the second direction is orthogonal to the first direction.

### ***Response to Arguments***

Applicant argues that claims 1-21 read on the embodiment of figure 1(b).

Although the embodiment of figure 1(b) recites "an alternative embodiment to that of FIG. 1(b) might have an additional level of buried elements, where the elements are located either in front of and/or behind the plane of the trench capacitor", this would be an embodiment that is patentably distinct from that of figure 1(b).

**Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722**

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**and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.**

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(571) 272-1660**. The Examiner is in the Office generally between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**

A handwritten signature in black ink, appearing to read 'Ori Nadav', with a stylized flourish at the end.

O.N.  
9/20/04

ORI NADAV  
PRIMARY EXAMINER  
TECHNOLOGY CENTER 2800